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Description

METHOD FOR FABRICATING SHALLOW TRENCH ISOLATION BETWEEN DEEP TRENCH CAPACITORS

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a method for fabricating shallow trench isolation (STI) between deep trench capacitors and, more particularly, a logic-process compatible method for fabricating shallow trench isolation (STI) between deep trench capacitors of trench-capacitor dynamic random access memory (DRAM) devices.

[0003] 2. Description of the Prior Art

[0004] Trench-capacitor DRAMdevices are known in the art. Typically, a trench-storage capacitor consists of a very-high-aspect-ratio contact-style hole pattern etched into the substrate, a thin storage-node dielectric insulator, a doped low-pressure chemical vapor deposition (LPCVD)

polysilicon fill, and buried-plate diffusion in the substrate. The doped LPCVD silicon fill and the buried plate serve as the electrodes of the capacitor. A dielectric isolation collar in the upper region of the trench prevents leakage of the signal charge from the storage-node diffusion to the buried-plate diffusion of the capacitor. After forming the trench capacitors, shallow trench isolation (STI) regions are formed on the substrate between the trench capacitors.

[0005] Generally, the prior art STI process for trench capacitor DRAM devices includes the following main steps:

[0006] 1.Deep trench (DT) process;

[0007] 2.Cap hard mask layer deposition and patterning;

[0008] 3.Hard mask etching and photoresist strip;

[0009] 4.STI trench etching and hard mask strip; and

[0010] 5.STI gap fill and planarization.

[0011] Referring to Fig.1 to Fig.5 of schematic cross-sectional views showing the fabrication of STI regions between trench capacitors according to the prior art method. As shown in Fig.1, a semiconductor chip 1 comprising a logic area 11 and a memory array area 12 is provided. As indi-

cated, a plurality of trench capacitors 20 have been formed in the semiconductor substrate 10 within the memory array area 12 of the semiconductor chip 1. Typically, each of the trench capacitors 20 comprises a buried plate diffusion (not shown) acting as one electrode of the capacitor, a poly storage node 24 serving as the other electrode of the capacitor, and a node dielectric 22 between the two electrodes. A collar oxide layer 26 is formed on an upper portion of the deep trenches. A pad nitride layer14 laid over the semiconductor substrate 10 is typically used to define the openings of the deep trenches. At this stage, after forming the trench capacitor structures 20, there is a recess 28 left on each top of the trench capacitor structures 20.

[0012] As shown in Fig.2, a doped silicate glass layer 32 is deposited on the surface of the semiconductor chip 1. The doped silicate glass layer 32 has a thickness of about 3000 to 4000 angstroms. Typically, the doped silicate glass layer 32 is made of borosilicate glass (BSG) or borophosposilicate glass (BPSG). The doped silicate glass layer 32 covers the pad nitride 14 and fills the recesses 28.

[0013] As shown in Fig.3, a bottom anti-reflection coating (BARC)

34 is deposited on the doped silicate glass layer 32, followed by photoresist coating. A conventional lithographic process and subsequent baking process are then carried out to pattern the photoresist coating, thereby forming a photo mask 36 defining memory array area trench openings 43 and logic area trench openings 45 therein.

[0014] As shown in Fig.4, using the photo mask 36 as an etching mask, a plasma dry etching is performed to etch the BARC 34, the doped silicate glass layer 32, the pad nitride 14, the silicon substrate 10, a portion of the storage node 24, and a portion of the collar oxide 26 through the memory array area trench openings 43 within the memory array area 12, thereby forming isolation trenches 53, and to etch the BARC 34, the doped silicate glass layer 32, the pad nitride 14, the silicon substrate 10 through the logic area trench openings 45 within the logic area 11, thereby forming isolation trenches 55. Thereafter, the remaining photo mask 36, the BARC 34, and the doped silicate glass layer 32 are removed.Finally, as shown in Fig.5, the isolation trenches 53 and 55 are filled with gap fill dielectric 58 and planarized.

[0015] However, there are several problems with the above-described prior art STI method for trench capacitor DRAM

devices. First, the thick hard mask (doped silicate glass layer 32) leads to bad critical dimension (CD) uniformity and large iso/dense CD bias. Secondly, the STI trench recipe is difficult to develop because of the complex structure of the trench capacitor. Thirdly, the above-described prior art STI method for trench capacitor DRAM devices is not compatible with the logic processes.

SUMMARY OF INVENTION

[0016] Accordingly, the primary object of the present invention is to provide an improved STI method for trench capacitor DRAM devices to form STI between trench capacitors and such method is compatible with the logic processes.

[0017] According to one preferred embodiment of this invention, a method for fabricating shallow trench isolation (STI) between deep trench capacitors is disclosed. A semiconductor substrate having thereon a patterned pad layer is provided. The semiconductor substrate has a plurality of deep trench capacitors formed therein, each of which comprising a buried plate in the semiconductor substrate serving as one electrode of the deep trench capacitor, a storage node serving as the other electrode of the deep trench capacitor, a node dielectric layer between the buried plate and the storage node, and a collar oxide dis-

posed at an upper portion of the deep trench capacitor. A dielectric layer is filled into a capacitor top recess on each of the deep trench capacitors. The studded dielectric layer has a top surface that is coplanar with the pad layer. A buffer layer is deposited over the semiconductor substrate. A photo mask defining trench openings is formed over the buffer layer. A plasma etching process is performed to etch the buffer layer, the pad layer, and then etching into the semiconductor substrate selective to the dielectric layer and the collar oxide that both keep the deep trench capacitors intact through the trench openings, thereby forming isolation trenches between the deep trench capacitors. After stripping the photo mask, the isolation trenches are filled with gap filling material.

[0018] Other objects, advantages, and novel features of the claimed invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

Brief Description of Drawings

[0019] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, to-

gether with the description, serve to explain the principles of the invention. In the drawings:

[0020] Fig.1 to Fig.5 are schematic cross-sectional views showing the fabrication of STI regions between trench capacitors according to the prior art method; and

[0021] Fig.6 to Fig.11 are schematic cross-sectional views showing the fabrication of STI regions between trench capacitors according to one preferred embodiment of the present invention.

DETAILED DESCRIPTION

[0022] Referring to Fig.6 to Fig.11 of schematic cross-sectional views showing the fabrication of STI regions between trench capacitors according to one preferred embodiment of the present invention, in which like reference numerals designate similar or corresponding elements, regions, and portions. As shown in Fig.6, a semiconductor chip 1 comprising a logic area 11 and a memory array area 12 is provided. As indicated, a plurality of trench capacitors 20 have been formed in the silicon substrate 10 within the memory array area 12 of the semiconductor chip 1. Each of the trench capacitors 20 comprises a buried plate diffusion (not shown) serving as one electrode of the capacitor, a poly storage node 24 serving as the other electrode

of the capacitor, and a node dielectric 22 between the two electrodes. A collar oxide layer 26 is formed on an upper portion of the deep trenches. A pad nitride layer14 laid over the semiconductor substrate 10 is used to define the openings of the deep trenches. At this stage, after forming the trench capacitor structures 20, there is a recess 28 (capacitor top recess) left on each top of the trench capacitor structures 20.

[0023] As shown in Fig.7, dielectric layer (not shown) is deposited over the semiconductor chip 1. The dielectric layer, preferably an HDPCVD oxide layer formed by conventional high-density plasma chemical vapor deposition (HDPCVD) methods, is then polished by CMP stopping on the pad nitride 14, thereby leaving the remaining dielectric layer 62 studded in the recesses 28 on the trench capacitors 20. The remaining dielectric layer 62 studded in the recesses 28 has a top surface that is substantially coplanar with the surrounding pad nitride 14. At this phase, the semiconductor chip 1 has a planar topography.

[0024] As shown in Fig.8, a buffer layer 64 is then deposited over the semiconductor chip 1. The buffer layer 64, which covers the studded dielectric layer 62 and the pad nitride 14, has a relatively thinner thickness of about 500 angstroms

comparing with the prior art method. According to the preferred embodiment of this invention, the buffer layer is made of silicon nitride or silicon oxynitride (SiON), preferably silicon nitride, but not limited thereto.

[0025] As shown in Fig.9, a bottom anti-reflection coating (BARC) 34 is deposited on the buffer layer 64, followed by photoresist coating. A conventional lithographic process and subsequent baking process are then carried out to pattern the photoresist coating, thereby forming a photo mask 36 defining memory array area trench openings 43 and logic area trench openings 45 therein. It is noted that, in another embodiment, the BARC 34 may be omitted.

[0026] As shown in Figs. 9 and 10, using the photo mask 36, the studded dielectric layer 62, and the collar oxide 26 as an etching mask, a plasma dry etching is performed to etch the BARC 34, the nitride buffer layer 32, the pad nitride 14, and the silicon substrate 10 through the memory array area trench openings 43 and the logic area trench openings 45 selective to the oxide dielectric layer 62 and the collar oxide 26, thereby forming isolation trenches 53 and 55, respectively. As indicated, the resultant isolation trenches 53 within the memory array area 12 have an approximately T-shaped cross section. This is because the

plasma dry etching uses a plasma recipe selective to the oxide dielectric layer 62 and the collar oxide 26 that protect the trench capacitors 20 during the etching. Thereafter, the photo mask 36 and the BARC 34 are removed.

[0027] Finally, as shown in Fig.11, the isolation trenches 53 and 55 are filled with gap fill dielectric 58 and planarized.

[0028] To sum up, the present invention studs oxide dielectric 62 into trench capacitor top recesses 28 after the formation of the trench capacitor structures 20. A cap buffer nitride 64 is then deposited over the substrate 10. The studded oxide dielectric 62 and the collar oxide 26 protect the trench capacitor during the subsequent selective dry etching, thereby forming isolation trenches having an approximately T-shaped cross section within the memory array area of the semiconductor chip 1. The present invention avoids the use of thick doped-silicate glass hard mask 32, thereby controlling the CD uniformity. Further, the recipe of STI trench etching is easy to control since the etching is selective to oxide dielectric 62 and the collar oxide 26, and the etching of complex capacitor structure 20 is avoided. Moreover, the present invention method is compatible with the logic processes.

[0029] Those skilled in the art will readily observe that numerous

modifications and alterations of the present invention method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.